

ECE 128 Lab – Syllabus Spring 2009

Week 1 – 1/12/09

-Verilog Introduction (Behavioral vs. structural)

1/19 – Martin Luther King Jr. Day – class canceled

Week 2 – 1/26/09

-VerilogA introduction

Week 3 – 2/2/09

-Synopsys – synthesis with standard cell intro

2/09/09 – class canceled

2/16/09 – President's Day

Week 4 – 2/23

-Synopsys – tetraMax/automatic test plan generation

- exporting 126 design from cadence to verilog

- test case generation for that exported verilog

-HW: generate test vectors for 126 design (from exported verilog) –for use with logic analyzer

3/4/09 – HW 2 DUE (postponed from 2/25)

Week 5 – 3/4 (snow day 3/2, make up 3/4 ---during full lecture – long lab)

-Synopsys->Cadence – Place & Route

-Verilog Review

-blocking vs. non-blocking

-test benches – how to test all possibilities of input using for loop

-print & \$monitor statements to get lists of all inputs

-Project Introduction – Overview –ALU, PC, CU, IO & DAC/ADC

-organizing files

-running test bench

-Digital Implementation: **PC** in verilog, testing w/ tb

-synthesizing

-HW: implement PC, synthesize in standard cells

Week 6 – 3/9

-Digital Implementation: **CU** unit in verilog

-Discussion on synthesizable state machines?

-HW: implement CU (over break) synthesize in standard cells

3/11/09 – HW 3 DUE

3/16 – 3/21 – Spring Break

Week 7 – 3/23

-Project Continuation: Digital portion

-Digital Implementation: (ALU) Control Unit in verilog

-how to write a synthesizable state machine

-Digital Implementation: IO unit

-HW: implement ALU & IO, synthesize in standard cells

Week 8 – 3/30

- Project Continuation: VerilogAMS introduction
- Cadence AMS Implementation: ADC
- Cadence AMS Implementation: DAC
- Cadence AMS Configuration Hierarchy Editor Introduction
- HW: Place and Route CPU

Week 9 – 4/6 (MOSIS CHIPS SHIP ON APRIL 9TH)

- Logic Analyzer/HiLEVEL machine Demo
- How to use Camera in VLSI lab to take picture of chip
- HW: “NAND/FLIP/FLOP” chips to students

Week 10 – 4/13

- Project Continuation: Tying Digital (verilog) and Analog (verilog-ams) together
- importing verilog into cadence
- creating DAC – CPU – ADC control module – reading in memory instructions from file
- creating DAC – CPU – ADC test bench

Week 11 – 4/20

- Project Work
- HW: complete ECE 126 chip testing

4/22 – Professor Zaghoul to visit lab?

Week 12 – 4/27 (Last lab before final presentations are due)

- Project Work

Week 13 – 4/29 – GWU Makeup Monday class

4/29 – ECE 128 – Final Report Day (ECE 126 Chips must be fully tested, CPU/AMS project must be completed, laid out, and fully tested)

4/30 – Make up classes at GWU

May 4-12 – Final Exam Days at GWU

May 6, 2009 – (5:20-7:20pm) Tompkins 309 – FINAL EXAM