

## **ECE 126 – Fall 2009 – Lab Schedule**

Lab: 9/1/09 – Mosis NDA, Configure Env, Cadence Inverter Schematic + symbol

Lab: 9/8/09 – CMOS Inverter Transient Analysis, Parameteric Analysis, VTC

Lab: 9/15/09 – CMOS Inverter Layout – Part 1

Due: **HW # 1**

Lab: 9/22/09 – CMOS Inverter Layout – Part 2, DRC, Extraction, LVS, BackAnnotation

Lab: 9/29/09 – Project Overview, Interconnecting Instanced Cells, Basic Routing

Due: **HW #2**

Lab: 10/6/09 – Back Annotating vs. Simulating off Extracted View & Q1

**Lecture: 10/12/09 – Project Proposal Due**

Lab: 10/13/09 – Dynamic Logic in Cadence

Due: **HW #3**

Lab: 10/20/09 –Power Dissipation in Cadence, Interconnect Modeling, PAD Load Cap

**Lecture: 10/26/09 – Midterm Exam**

Lab: 10/27/09 – Creating a verilog test bench

**HW #4 – Due 10/30/09 (FRIDAY - ELECTRONIC)**

Lab: 11/3/09 – Sequential Logic – Sharing Project Code between partners

Due: Complete Project *Schematic* on Paper (**Graded**)

Due: Test Strategy Explained (**Graded**)

Lab: 11/10/09 – Importing PAD Frame (GDS2) & simulating project with it

Due: Project Schematic in Cadence (**Graded**)

Due: Project Test Strategy implemented in schematic (**Graded**)

**HW #5 Due**

Lab: 11/17/09 – Exporting GDS2, re-importing, & re-testing

Due: Project Layout for sub-modules (**Graded**)

Due: Project Layout for test-modules (**Graded**)

Lecture: 11/23/09 – Professor Zaghoul visits *lab* to see project progress

Lab: 11/24/09 – Project Review / Help

**HW #6 Due**

11/26->11/27 – Thanksgiving Break (Good time to work on project)

Lecture: 11/30/09 – Professor Zaghoul visits *lab* to see project progress

Lab: 12/1/09 – Final Lab Date

Due: Complete Project Layout (without pad frame) (**Graded**)

Due: Written & Oral Report Outline (in PowerPoint) (**Graded**)

**Lecture: 12/7/09 – Last Day of Classes - Project Due Date – Oral & Written**

12/9/09 ->12/10/09 – Reading Days

12/11/09 -> 12/19/09 – Final Exam Period

**Lecture: 12/14/09 – Final Exam**