

RESUME

Bhagirath Narahari

EDUCATION

- **Ph.D.**, Computer and Information Science, 1987
University of Pennsylvania, Philadelphia
Thesis: An Integrated Analysis of Algorithms and Interconnection Networks.
- **MS**, Computer and Information Science, 1984
University of Pennsylvania, Philadelphia.
- **B.E.(hons.)** Electrical and Electronics Engineering, 1982
Birla Institute of Technology & Science, Pilani, India.

EXPERIENCE

- **Department Chair:** July 1999 – 2002
Dept. of Computer Science,
The George Washington University, Washington,DC
- **Professor:** July 1, 2000 – present.
Dept. of Computer Science,
The George Washington University, Washington,DC
- **Associate Professor:** July 1, 1999 – June 30, 2000.
Dept. of Computer Science,
The George Washington University, Washington,DC
- **Associate Professor:** September 1993 –99.
Dept. of Electrical Engineering and Computer Science,
The George Washington University, Washington,DC

- **Visiting Scientist:** June 1999
ReaCT-ILP Laboratory
Courant Institute of Mathematical Sciences
New York, NY
- **Curriculum Coordinator (Computer Engineering):** September 1997–99.
Dept. of Electrical Engineering and Computer Science,
The George Washington University, Washington,DC
- **Research Scientist:** July 1995
Computer Technology Institute
Patras, Greece
- **Research Scientist:** August 1994 – Dec. 1994
The New York State Center for Advanced Technology in Computer Applications and
Software Engineering (CASE Center)
Syracuse University, Syracuse, NY 13244
- **Assistant Professor:** September 1987 – August 1993.
Dept. of Electrical Engineering and Computer Science,
The George Washington University, Washington,DC
- **Visiting Scientist:** August 1993.
Institute for Computer Applications in Science and Engineering,
NASA Langley Research Center, Hampton, Virginia.
- **Visiting Research Scientist:** July – August 1992.
School of Computing Science, Simon Fraser University, Burnaby, BC, Canada.
- **Research Assistant:** Jan. 1983 – August 1987.
Dept. of Computer and Information Science, University of Pennsylvania, Philadelphia,
Pennsylvania.
- **Engineer(Trainee):** Jan. 1982 – July 1982.
Department of Electronics, Government of India, New Delhi, India.

RESEARCH INTERESTS

Embedded Systems, Computer Architecture, Compiler Optimization, Instruction Level Parallel Processors, Real-time computing environments, Parallel and Distributed Processing, Scheduling theory, Wireless and Sensor Networks, Database Management systems, Multimedia Information retrieval systems.

GRANTS AND AWARDS

- “Home of the 21st Century”, with S. Rotenstreich, C. Korman, R. Simha, R. Lindeman, S. Ahmadi, America Online, 2002-2003.
- “Wireless Infrastructure”, NSF Major Research Infrastructure Grant, 2002.
- “Connectivity Laboratory”, America Online, 2001.
- “AOL Smart Home”, with S. Rotenstreich, C. Korman, R. Lindeman, R. Simha, America Online, 2001.
- “Optimizing Assembler for EPIC/VLIW Architectures:Phase 3”, NSA-LUCITE, (Dec.2000–May 2002).
- “Electronic Commerce Coursework”,co-PI with Rahul Simha, Rob Lindeman and R. Heller, National Science Foundation. (2000-2003).
- “Power Aware Computing Toolset (PACT): A Software Infrastructure for Embedded Systems Design”, NASA, co-PI with R. Simha and Intelligent Automation Inc., 1999-2001.
- Equipment grant from Intel Corp - Beta Version of the Itanium Processor, to support research in EPIC/VLIW Architectures.
- “Optimizing Assembler for EPIC Processors: Phase 2”, NSA-LUCITE Program, 1999-2000.
- “Optimizing Assembler for VLIW Architectures: Phase 1”, NSA-LUCITE program, (March – Nov. 1999).
- “Embedded Systems Laboratory”, NSA- Equipment Grant, Feb. 1999.
- “Software Design for Real-time Systems on Parallel Computers: Specification and Verification”, co-PI with Profs. Choudhary and Gehlot, Rome Air Force Laboratories, Rome, NY, Grant Amount: \$100,000, (June 1994- June 95).
- *NSF Research Initiation Award*, 1992–1995
“Processor Allocation on Partitionable Parallel Architectures”, National Science

Foundation Research Initiation Award, Division of Computer and Computation Research Grant No. CCR-9209345, Grant Amount: \$90,000; Duration: 3 years (1992–1995).

- *University Facilitating Fund, 1992*
“Processor Allocation Problems in Parallel Processing”, The George Washington University, University Committee on Research, Grant Amount \$ 7440; Jan.1992–Dec. 1992.
- *University Facilitating Fund, 1991*
“A New Approach for Mapping Parallel Programs to Parallel Architectures”, The George Washington University, University Committee on Research, Grant Amount \$ 7440; July 1991– Oct. 1991.
- *University Facilitating Fund, 1990*
“A Parallel Processing Approach Using Parallel Primitives” The George Washington University, University Committee on Research, Grant Amount \$ 8440; July 1990– Oct. 1990.
- *University Facilitating Fund, 1989*
“A Knowledge Driven Approach for Efficient Execution of Tasks on Partitionable Parallel Architectures”, The George Washington University, University Committee on Research, Grant Amount \$ 8440; June 1989 – Sept. 1989.

PUBLICATIONS

Journal Publications:

1. “A real-time parallel scheduler for the imprecise computations model”, H. Foad (doctoral student), B. Narahari and J. Hahn), *Journal of Parallel and Distributed Computing Practices*, Vol.2, No.1, 2000.
2. “Routing and scheduling I/O transfers in mesh networks”, B. Narahari, S. Shende, R. Simha, and S. Subramanya (doctoral student), in *Journal of Parallel and Distributed Computing*, Vol.57, No.1, April 1999.
3. “Efficient Algorithms for Erasure Node Placement on Slotted Dual Bus Networks”, B. Narahari, R. Simha and S.Shende, *IEEE/ACM Trans. Networking*, Vol. 4, No. 5, 1996, pp. 779-784.

4. "On Partitioning Grid Structured Parallel Computations", B. Narahari and R. Simha, *Journal of Combinatorial Mathematics and Combinatorial Computing*, Vol.21,pp. 3–24, June 1996.
5. "An Approximation algorithm for preemptive scheduling on parallel task systems", R. Krishnamurti and B. Narahari, *SIAM Journal on Discrete Mathematics*, pp. 661–669, Nov. 1995.
6. "Optimal processor assignment for pipelined series-parallel computations", A. Choudhary, B. Narahari, D.M. Nicol and R. Simha, *IEEE Transactions on Parallel and Distributed Systems*, Vol.5, No.4, pp. 439–445, April 1994,
7. "Computing sum of vectors on rings, meshes and hypercubes", B. Narahari and P. Papaioannou (graduate student), *ISMM International Journal of Mini and Micro Computers*, Vol. 16, No. 3, pp. 109–118, April 1994.
8. "Efficient Algorithms for Mapping and Partitioning a Class of Parallel Computations", H.-A. Choi and B. Narahari, in *Journal of Parallel and Distributed Computing*, 19, 349–363, (1993).
9. "Allocating Program Modules to Processors in a Distributed System" L. Tao, B. Narahari, and Y. Zhang (graduate student), in *Journal of Combinatorial Mathematics and Combinatorial Computing*, Vol. 14, 97–135 (Sept. 1993).
10. "An Efficient Heuristic Scheme for Dynamic Remapping of Parallel Computations", Alok Choudhary, B. Narahari, and R. Krishnamurti, *Parallel Computing*, Vol. 19 no. 6, (June 1993), 621–632.
11. "Assigning Optimal Configurations to Task Precedence Graphs" H-A. Choi and B. Narahari, *The Journal of Combinatorial Mathematics and Combinatorial Computing*, Vol. 13, (April 1993), 77–96.
12. "Mapping a Chain Task to Chained Processors" Y. Han, B. Narahari and H-A Choi, in *Information Processing Letters*, Vol. 44, No. 3, (1992), 141–148 (Nov. 1992).
13. "Optimal Single Path Routing with Delays" R.Simha and B. Narahari, *Computer Networks and ISDN Systems*, Vol. 24, pp. 405–419, June 1992,
14. "Mapping Binary Precedence Trees to Hypercubes" S. Ullman (doctoral student) and B. Narahari, in *Parallel Processing Letters*, Vol.2, No.1, pp. 81–88, March 1992.
15. "Optimal Subcube Assignment in Partitionable Hypercubes" R. Krishnamurti and B. Narahari, *Parallel Processing Letters*, Vol.2, No.1, pp. 89–96, March 1992.

16. “Optimal Embedding of Torus in Rings” Y-W.E. Ma, B. Narahari and L.Tao, in *Information Processing Letters*, Vol. 41, pp. 227-231, March 1992.
17. “Topological Properties of Generalized Banyan-Hypercube Networks”
A. Youssef and B. Narahari, *Journal of Parallel and Distributed Computing*, Vol. 14, No.1, pp.98–103, Jan. 1992
18. “Banyan-Hypercube Networks”, A. Youssef and B. Narahari, *IEEE Transactions on Parallel and Distributed Systems*, Vol.1, No. 2, pp.160–169, April 1990.

Refereed Conference Publications:

1. “Application specific memory partitioning for Low Power”, S. Udayakumaran, B. Narahari, R. Simha, *Proc. of Workshop on Compiler and Operating Systems for Low Power, COLP 2002*, Sept. 2002.
2. Y.L. Chobe, B. Narahari, R. Simha, W-F. Wong, “Tritanium: An IA-64 Code Generator for the Trimaran Compiler Infrastructure”, in *1st IEEE EPIC Workshop, held in Conjunction with MICRO*, Dec. 2001.
3. “Memory issues in power-aware design of embedded systems:An overview”, R. Levy, B. Crilly (doctoral students), B. Narahari and R. Simha, *2nd Workshop on Compiler and Architecture Support for Embedded Systems*, October 1-3, 1999.
4. “Fine grained register allocation for EPIC processors with predication”, H.Kim (doctoral student), K. Gopinath, V. Kathail and B. Narahari, *Proc. Parallel and Distributed Processing Techniques and Applications, PDPTA-99*, Las Vegas, 1999.
5. “Use of transforms in indexing in audio databases”, S. Subramanya (doctoral student), A. Youssef, B. Narahari and R. Simha, *Proc. International Conference on Computational Intelligence and Multimedia Applications*, New Delhi, India, Sept. 1999.
6. “I/O Performance of X-Y routing in 2-D Meshes under various disk load balancing schemes”, S. Subramanya (doctoral student), B. Narahari and R. Simha, *Proc. International Conference on Parallel and Distributed Computing Systems (PDCS-99)*, Ft. Lauderdale, Florida, August 1999.
7. “I/O Performance of X-Y routing in 2-D Meshes under various Node-to-Disk Assignments”, S. Subramanya (doctoral student), B. Narahari and R. Simha, *Proc. International Conference on Computers and Their Applications*, Cancun, Mexico, April 1999.

8. "Automated classification of audio data and retrieval based on audio classes", S. Subramanya (doctoral student), A. Youssef, B. Narahari and R. Simha), *Proc. International Conference on Computers and Their Applications*, Cancun, Mexico, April 1999.
9. "Dynamic load balancing schemes for computing accessible surface area of protein molecules" E. Suh (doctoral student), B. Narahari and R. Simha, *International conference on High Performance Computing*, December 1998.
10. "Placement of storage nodes in a network", S. Subramanya (doctoral student) and B. Narahari, *Proc. Parallel and Distributed Techniques and Applications, PDPTA*, 1998.
11. "Scheduling I/O Transfers in a 2-D Mesh with Packet Deadlines", S. Subramanya (doctoral student) and B. Narahari, *Proc. 36th Annual Southeast Conference*, ACM Press, Marietta, Georgia, April 1998.
12. "Parallel Real-time systems: Formal Specification", A. Choudhary, V. Gehlot and B. Narahari, *Proc. IEEE International Conference on High Performance Computing*, December 1997, IEEE Computer Society Press.
13. "Algorithms for mapping task graphs to a heterogeneous network of workstations" H-A. Choi, B. Narahari and R. Simha), *Proc. of ADCOMP 97: Fifth International Conference on Advanced Computing*, Chennai, India, Dec. 1997.
14. "Transform-based indexing of audio data for multimedia databases", R. Simha, S. Subramanya (doctoral student), B. Narahari, and A. Youssef, *International Conference on Multimedia Computing and Systems*, Ottawa, Canada, June 1997.
15. "File Allocation for a Parallel Webserver", H-A. Choi, B. Narahari and R. Simha, *Int. Conf. High Performance Computing*, (IEEE Computer Society Press), December 1996, Trivandrum, India.
16. "Processor Allocation on Partitionable Architectures" B. Narahari and R. Krishnamurti, in *Proceedings of International Conference on High Performance Computing*, Delhi, India, December 1995, in *High Performance Computing*, Tata McGraw-Hill, 279–284.
17. "Routing and Scheduling I/O Transfers on Wormhole Routed Mesh Networks" B. Narahari, S. Shende, R. Simha, and S. Subramanya (doctoral student), in *Proceedings of International Conference on High Performance Computing*, Delhi, India, December 1995, in *High Performance Computing*, Tata McGraw-Hill, 779–784.

18. "Efficient Algorithms for Erasure node placement on DQDB networks" B. Narahari, R.Simha and S. Shende, *Proceedings of International conference on Communucations, ICC '95*, Seattle, June 1995, pp. 935-939.
19. "A Specification language for Parallel Real-time systems" A. Choudhary, V.Gehlot, B. Narahari, M. Benincasa, and R. Metzger, in *Proceedings of Third workshop on Parallel and Distributed Real-time Systems*, IEEE Computer Society Press, Santa Barbara, CA, April 1995, pp. 165-173.
20. "PRETSEL: Parallel Real-Time Specification Language", A. Choudhary, V. Gehlot and B. Narahari, *Proceedings of First International Workshop on Parallel Processing*, Bangalore, India, Dec. 1994, pp.509-514.
21. "Algorithms for Efficient Partitioning of Parallel Computations", B. Narahari and R. Simha, *Proceedings of First International Workshop on Parallel Processing*, Bangalore, India, Dec. 1994, pp. 271-275.
22. "Matching and Scheduling in a Generalized Optimal Selection Theory", H-A. Choi, B. Narahari, and A. Youssef, *Third Workshop on Heterogeneous Computing*, April 1994.
23. "Heuristics for Mapping Parallel Computations to Heterogeneous Parallel Architectures", L. Tao, B. Narahari and Y.C. Zhao (graduate student), *Proc. of Second Workshop on Heterogeneous Processing, HP '93*, 36-41, Newport Beach, California, April 13-16, 1993.
24. "Scheduling Independent Tasks on Partitionable Hypercube Multiprocessors", B. Narahari and R. Krishnamurti, *Proc. of 7th International Parallel Processing Symposium*, pp. 118-122, Newport Beach, California, April 13-16, 1993.
25. "Parallel Computation of Solvent Accessible Surface Area of Protein Molecules", with E. Suh (doctoral student), B.K. Lee, B. Narahari and Alok N. Choudhary, *Proc. of 7th International Parallel Processing Symposium*, pp. 685-689, Newport Beach, California, April 13-16, 1993.
26. "Efficient Heuristics for Task Assignment in Distributed Systems", L. Tao, B. Narahari and Y.C. Zhao, in *Proc. of ICPADS'92 - 1992 International Conference on Parallel and Distributed Systems*, HsinChu, Taiwan, December 16-18, 1992.
27. "Algorithms for Scheduling Independent Jobs on Partitionable Hypercubes" R. Krishnamurti and B. Narahari, in *Proc. of The Fourth Symposium on the Frontiers of Massively Parallel Computation*, pp. 543-544, McLean, Virginia, October 1992.

28. “Preemptive Scheduling on Partitionable Parallel Architectures”, R. Krishnamurti and B. Narahari in *Proc. 1992 International Conference on Parallel Processing*, Vol.1, pp. 268–275, St. Charles, Illinois, August 1992.
29. “Mapping a Chain task to chained processors”, Y. Han, B. Narahari , and H-A. Choi in *4th International Conference on Computing and Information*, Toronto, Canada, May 1992, pp. 176-177.
30. “Allocating Partitions to Task Precedence Graphs”, H-A. Choi and B. Narahari, *Proc. 1991 International Conference on Parallel Processing*, Vol.1, pp. 621–624, St. Charles, Illinois, August 1991.
31. “Algorithms for Mapping and Partitioning Chain Structured Computations”, H.-A. Choi and B. Narahari, *Proc. 1991 International Conference on Parallel Processing*, Vol.1, pp. 625–628, St. Charles, Illinois, August,1991..
32. “Scheduling Precedence Graphs to Minimize Total System Time on Partitionable Parallel Architectures”, H.-A. Choi and B. Narahari, *Proc. of the Second IEEE Symposium on Parallel and Distributed Processing*, pp. 407–410, Dallas, Texas, December 1990.
33. “Mapping Binary Precedence Trees to Hypercubes and Meshes”, Stuart Ullman (doctoral student) and B. Narahari, *Proc. of the Second IEEE Symposium on Parallel and Distributed Processing*, pp. 838–841, Dallas, Texas, December 1990.
34. “Topological Properties of Banyan-Hypercube Networks”, A. Youssef and B. Narahari, *Proc. of the 3rd Symposium on the Frontiers of Massively Parallel Computation*, pp. 324–332, October, 1990.
35. “Scheduling Precedence Graphs to Minimize Completion Time on Partitionable Parallel Architectures”, H.-A. Choi and B. Narahari, *Proc. of the 28th Annual Allerton Conference on Communication, Control and Computing*, pp. 272–273, October 1990.
36. “Computing Sum of Vectors on Rings, Meshes, and Hypercubes”, B. Narahari and P. Papaioannou (graduate student), *ISMM Conference on Parallel and Distributed Computing and Systems*, pp.375–378, October, 1990.
37. “A Framework for Evaluating Communication Structures of Parallel Algorithms” B. Narahari and P.Papianoannou (graduate student), *Proc. of The Fourth Annual Parallel Processing Symposium*, pp. 499–512, April 1990.

38. "Scheduling on Parallel Processing Systems Using Parallel Primitives", H-A Choi, B. Narahari, S. Rotenstreich, and A. Youssef), in *PARBASE-90: Two track International Conference on Databases, Parallel Architectures and their Applications*, pp. 56–65, Florida, March 1990.
39. "A Methodology for Matching Parallel Algorithms and Interconnection Networks", B. Narahari, *Proc. of ISMM International Symposium on Intelligent Distributed Processing*, Ft. lauderdale, Florida, December 1989.
40. "A Framework for a Portable, Intelligent Operating System for Parallel Machines", N. Alexandridis, H-A Choi, B. Narahari, S. Rotenstreich, A. Youssef, and C. Kolli (graduate student), *Proc. of the ISMM International Symposium on Intelligent Distributed Processing*, pp. 14–17, Ft. lauderdale, Florida, December 1989.
41. "A Software Environment of Architecture Prototypes for Evaluating Parallel Vision Systems and Algorithms," N. Alexandridis, P. Papaionnou (graduate student), B. Narahari and A. Youssef, *Proc. of the First IEEE International Workshop on Tools for Artificial Intelligence*, pp. 518–525, Washington, DC, October 1989.
42. "A Parallel Primitives Approach to Parallel Programming," S. Rotenstreich, B. Narahari and A. Youssef, *Proceedings of the 12th Minnowbrook Workshop: Software Engineering for Parallel Computing*, New York, July 1989.
43. "Routing, Embedding and Partitioning on the Banyan-Hypercube Network," A. Youssef and B. Narahari, *Proceedings of The First Annual IEEE Symposium on Parallel and Distributed Computing*, pp. 383–384, Dallas, May 1989.
44. "A Hierarchical, Partitionable, Knowledge Based Parallel Processing System," N. Alexandridis, H-A Choi, B. Narahari, S. Rotenstreich, and A. Youssef, *Proc. of the Third Annual Parallel Processing Symposium*, pp. 843–859, Fullerton, California, March 1989.
45. "The Banyan-Hypercube Network - A Synthesis of Banyans and Hypercubes," A. Youssef and B. Narahari, *Proc. of the Third Annual Parallel Processing Symposium*, pp. Fullerton, California, March 1989.
46. "Reconfigurable Special-Purpose Computers", Y.W.Ma, R. Krishnamurti, B. Narahari, D.G. Shea, L.Tao, and R. Varadarajan, *Proc. of the Second International Conference on Supercomputing*, pp. 343–351, May 1987.
47. "Optimal Mappings between Interconnection Networks for Performance Evaluation", Y.W. Ma and B. Narahari, in *Proc. of the The 6th International Conference on Distributed Computing Systems*, pp. 16–25, June 1986.

Book Chapters:

1. “Parallel Computer Architectures”, R. Krishnamurti and B. Narahari, in *Handbook of Statistics, Vol.9: Computational Statistics*, pp. 69–99. edited by C.R. Rao, North-Holland (Elsevier Science Publishers), Amsterdam, The Netherlands, 1993.
2. “Scheduling on Parallel Processing Systems Using Parallel Primitives”, (with H-A. Choi, S. Rotenstreich and A. Youssef) in *Parallel Architectures*, Editors: N. Rishé and S. Navathe, IEEE Computer Society Press, 1991, pp. 88–107.
3. “High Performance Special-Purpose Computer Architectures for Robotic Sensing”, (with Y-W.E. Ma, R. Krishnamurti, D.G. Shea, and K.Shu) in *Specialized Computer Architectures for Robotics and Automation*, editor: J. Graham, publisher: Gordon and Breach of N.Y. 1987.

TEACHING and CURRICULUM DEVELOPMENT

- **Courses Taught at GWU:**

Embedded Systems, Parallel Computer Architectures, Advanced Computer Architectures, Database Management, Compiler Optimization, Database Systems, Advanced Information Systems, Theory of Computation, Discrete Structures for Computer Science, Automata and Formal Languages, Topics in Parallel Processing.

PROFESSIONAL ACTIVITIES

- **Technical Support for Trimaran Compiler Infrastructure:** The embedded systems subgroup of the HACC laboratory is currently helping with technical support of the Trimaran infrastructure (www.trimaran.org).

- **Referee:**

Journal of Parallel and Distributed Computing, (Journal of) Parallel Computing, Information Processing Letters, IEEE Transactions on Computers, IEEE Computer, Parallel Processing Letters, IEEE Transactions on Parallel and Distributed Computing, Annual International Conference on Parallel Processing, International Conference on Distributed Computing Systems, International Parallel Processing Symposium, IEEE Symposium on Parallel and Distributed Computing, ISMM Conference on Parallel and Distributed Computing and Systems, Symposium on Frontiers of Massively Parallel Computation.

- **Program Committee:** IEEE 1999 International Conference on High Performance Computing (HIPC'99).
- **Local arrangements chair:** Second Workshop on Compiler and Architecture Support for Embedded Systems (CASES99) , 1999.
- **Local Arrangements Chair,** First Workshop on Compiler and Architecture Support for Embedded Systems (CASES 98), 1998.