



Figure 1: Precedence Graph/Dataflow graph

### Homework 5 Solutions

**Ques.1:**

First, assign labels to each instruction as shown below. The dataflow/precedence graph is shown in the figure. Since Load and Mult take 2 cycles, the critical path is BDF or ACEF. Shown in the figure is one sample rank function where the ranks are shown next to each node. Given this ranking, the priority list is  $\{B, D, F, A, C, E, G\}$ .

- A load R1, (R6)
- B load R0, (R7)
- C add R2, R1, R0
- D mult R3, R1, R0
- E add R4, R2, R0
- F mult R5, R3, R4
- G add R6, R2, R1

(a) Scheduling on a scalar processor with one execution unit. Let's assume that the units are not pipelined – i.e., we will have to wait 2 cycles after issuing a Load or Mult before we can issue anything into the units.

(b) Scheduling on an ILP processor is also shown in the same table; the schedule of each functional unit is shown. If we assume that the Load functional unit is a 2 stage pipeline (for example), then a schedule for such a hardware is also shown in the figure.

The table shows the schedule generated using list scheduling, for the ranking function defined earlier, for each of the 3 cases. The leftmost column shows the time, the second column shows instructions scheduled into the execution unit for the scalar processor, and columns 3,4,5 show the schedule for the ILP processor without a pipelined Load unit while columns 6,7,8 show the schedule for the ILP processor with a 2-state pipelined Load unit.

Time	Scalar	Load-ILP1	ALU1-ILP1	ALU2-ILP1	Load-ILP2	ALU1-ILP2	ALU2-ILP2
1	B	B	-	-	B	-	-
2	B	B	-	-	A,B	-	-
3	A	A	-	-	A	-	-
4	A	A	-	-	-	D	C
5	D	-	D	C	-	D	E
6	D	-	D	E	-	F	G
7	C	-	F	G	-	F	-
8	E	-	F	-	-	-	-
9	F	-	-	-	-	-	-
10	F	-	-	-	-	-	-
11	G	-	-	-	-	-	-
12	-	-	-	-	-	-	-

Ques.2: Some of the useful optimizations are loop unrolling, blocking, function inlining, strength reduction.